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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,601	01/24/2006	Kenichiro Tanaka	P29101	2841

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GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191

EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
08/19/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
pto@gbpatent.com

Office Action Summary	Application No.	Applicant(s)	
	10/565,601	TANAKA ET AL.	
	Examiner	Art Unit	
	JOSEPH NGUYEN	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/6/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/06/2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. Patent No. 6,333,522) in view of Chen (U.S. Publication No. 2004/0026708) and further in view of Oohata (U.S. Publication No. 2003/0160258).

Regarding claim 1, Inoue et al. discloses, for example, in figure 7B a light emitting device formed depositing p type and n type nitride semiconductor layers comprising deposited p type and n type nitride semiconductor layers 35, 32; a semiconductor surface electrodes 5, 6 to apply currents into each of the semiconductor layers; an

insulating layer 39 which holds the semiconductor layers, said insulating layer comprising two surfaces; and mount surface electrodes 25a, 24 provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor surface electrodes 5, 6 are made; wherein one of the semiconductor layers 32 has a non-deposited area where the other semiconductor layer is not deposited; one of the semiconductor surface electrodes 6 is built up on the surface of the non-deposited area; via holes (the holes formed in element 39 wherein conductive elements 25a, 24 are formed) are made in the insulating layer 39 which electrically connect the semiconductor surface electrodes 5, 6 and the mount surface electrodes 25a, 24, the via holes are filled with solder or electric conductive paste (*col. 26, lines 52-56*); the semiconductor surface electrodes 5, 6, the insulating layer 39, and the mount surface electrodes 25a, 24 are built up in this order on one side of the deposited semiconductor layers 32, 35; and a surface the other surface of the deposited semiconductor layers 32, 35 is used as light emitting surface. See col. 6, lines 40-65.

Nevertheless, Inoue et al. does not disclose the mount surface electrodes being structured and arranged to mount the light emitting device onto a mounting substrate by using solder. However, Chen discloses in Fig. 1 a light emitting device comprising the mount surface electrodes 41 (in paragraph [0009] Chen teaches of a welding metal 41, which can function as “mount surface electrodes” herein) being structured and arranged to mount the light emitting device onto a mounting substrate 50 by using solder 60 so as to improve the inject current capability in a light emitting device (paragraph [0010]). In view of such teaching, it would have been obvious at the time of the present invention to

modify Inoue et al. by including the mount surface electrodes being structured and arranged to mount the light emitting device onto a mounting substrate by using solder so as to improve the inject current capability in a light emitting device.

Further, Inoue et al. does not disclose this light emitting surface emits light beams directly to outside from the semiconductor layers because there is a transparent sapphire substrate on which the semiconductor layers are formed. However, Oohata discloses in figure 1 a nitride base light emitting diode device comprising the semiconductor layers (1, 2, 3) wherein a surface of one side of the light emitting layers emits light beams (the arrow) directly to outside from the semiconductor layers. In view of such teaching, it would have been obvious at the time of the present invention to modify Inoue et al. and Chen by including the light emitting surface emitting light beams directly to outside from the semiconductor layers so as to manufacture a light emitting diode device in a cost reduction manner (paragraph [0009]).

Regarding claim 2, Oohata discloses in paragraph [0056] the insulating layer (4) is made of resin.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. and Chen and Oohata, and further in view of Lowery et al. (U.S. Patent No. 6,878,973).

Regarding claim 4, Inoue et al. discloses in figure 7B substantially all the structure set forth in claims 4 except for phosphor being provided on the surface of the semiconductor layer. However, Lowery et al. discloses in figure 2 a nitride light emitting

device comprising phosphor 17 is provided on a surface of the semiconductor layer 23 so as to reduce contamination of the light emitting diode by the phosphor material (Abstract). In view of such teaching, it would have been obvious at the time of the present invention to modify Inoue et al. and Chen and Oohata by including phosphor being provided on the surface of the semiconductor layer as to reduce contamination of the light emitting diode by the phosphor material.

Response to Arguments

5. Applicant's arguments filed on 08/06/2010 have been fully considered but they are not persuasive.

With respect to claim 1, applicant argues Inoue et al. discloses micro-bumps are made of solder or gold, but does not disclose “via holes filled with solder or electric conductive paste” as now recited in amended claim 1. However, as stated above, the via holes are the holes that are formed in the insulating layer 39 wherein conductive elements 25a, 24 are form (or filled in) as shown in figure 7B, and since conductive elements 25a, 24 (micro-bumps) are made of Au (electric conductive paste) and filled in the via holes, it can be considered that the via holes are filled with electric conductive paste. It is noted that there is no specific material recited for the claimed electric conductive paste such that Au, which is electric conductive material, can be construed as “electric conductive paste” herein. In other words, Inoue et al. discloses the via holes are filled with electric conductive paste. Further, applicant argues Inoue does not teach

or suggest a light emitting device including, amongst the combination of features, mount surface electrode being structured and arranged to mount the light emitting device onto a mounting substrate by using solder. However, as stated above, Chen discloses in Fig. 1 a light emitting device comprising the mount surface electrodes 41 (in paragraph [0009]), Chen teaches of a welding metal 41, which can function as "mount surface electrodes" herein) being structured and arranged to mount the light emitting device onto a mounting substrate 50 by using solder 60 so as to improve the inject current capability in a light emitting device (paragraph [0010]). As such, it would have been obvious at the time of the present invention to modify Inoue et al. by including the mount surface electrodes being structured and arranged to mount the light emitting device onto a mounting substrate by using solder so as to improve the inject current capability in a light emitting device. Therefore, the combination of Inoue et al. and Chen would disclose "mount surface electrode being structured and arranged to mount the light emitting device onto a mounting substrate by using solder".

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 8:30 am- 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for

the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/J. N./

Examiner, Art Unit 2815

/KENNETH A. PARKER/

Supervisory Patent Examiner, Art Unit